Integrated High-Voltage CMOS Mixed-signal Instrumentation System for OFET-based Gas Sensor

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Abstract—This paper presents the concept and experimental results of a mixed-signal instrumentation system featuring a high-voltage CMOS ASIC. This system is dedicated to operate an OFET-based gas sensor. It is composed of high-voltage amplifiers, used to bias the OFET, a low-voltage analog signal processing chain, a 12-bit $\Sigma\Delta$ ADC, a 5-bit DAC and a digital SoC. This FPGA-implemented SoC controls the whole system. In particular, it generates specific control signals of the OFET’s gate voltage. The high voltage supply is generated on-chip by means of dedicated charge pumps.

Keywords—mixed-signal instrumentation; high-voltage CMOS; gas sensor; FPGA SoC

I. INTRODUCTION (Heading 1)

Because of their large application potential, organic semiconducting material-based sensors have recently gained significant interest of the scientific community [1][2][3]. In particular, Zheng et al. have demonstrated that Organic FET (OFET) devices have low detection threshold to various polar vapors and can thus be used as chemical sensors [2]. Their high sensitivity could be advantageously exploited to develop efficient and mobile sensors that meet the growing demand in various application fields such as security, biology, health care.

Yet, to be efficient as gas sensors, OFETs usually need up to several volts or even tens of volts biasing. This high-voltage (HV) requirement is often looked on as an inhibitor to the use of fully integrated circuits as OFET biasing and conditioning systems. This is due to the fact that combining low and high voltages, and above all, generating HV supply on a same circuit is not banal.

In this paper we present a HV-CMOS technology integrated mixed-signal instrumentation system dedicated to operate OFET-based gas sensors. The underlying idea of this work is to increase the portability and ease of use of the sensor by generating on-chip the various required voltage levels from a single low-voltage (LV) supply. In section II, we first present the concept of using OFET devices as gas sensors in order to identify the required specifications of the presented system. Section III is dedicated to detail the system’s architecture. The first experimental results are presented in section IV and finally, we draw some conclusions in section V.

II. CONCEPT

A. OFET-based gas sensor

Fig. 1. Bottom gate, bottom contacts OFET sensor structure.

The structure of the bottom gate, bottom contacts OFET is presented in Fig. 1. A $675\mu\text{m}$ -thick n-type silicon substrate ($3\times 10^{17}/\text{cm}^3$) acts as the OFET’s gate and is separated from the active zone by a 230nm SiO_2 layer. The active zone is made of various organic semiconductors, deposited from solution (for instance P3HT or soluble C_{60} derivatives), that can easily conduct holes (P3HT), electrons (PC_{61}BM) or simultaneously both types of charge carriers (P3HT: PC_{61}BM blends or some ambipolar organic semiconductors). Further details concerning the elaboration of P3HT based OFETs can be found in [4].

Fig. 2. OFET response to various ethanol + N₂ concentrations [4].

The active zone interacts with polar vapors inducing changes in the carriers’ mobility, i.e. in the OFET’s channel current I_{DS} . Fig. 2 shows the measured response of one of our P3HT OFET samples to various ethanol and N₂ concentrations [5].

B. Operating principle

The strategy for detecting an analyte is based on the measuring of the exposed OFET's transfer characteristic (i.e. the channel current as a function of the source-to-gate voltage, $I_{DS} = f(V_{GS})$). Fig. 3 is an example of I_{DS} measurement extracted from one of our OFET samples [6]. It shows that the voltages required to ensure proper sensor operation can reach values as high as a few tens of volts. This is mainly due to the type and thickness of the gate oxide (230nm SiO_2), to the OFET's channel size, and size and to the organic semiconductor used. Lowering both the source-to-gate and the source-to-drain voltages (V_{GS} and V_{DS} respectively) reduces I_{DS} and thus impacts the sensor's sensitivity. For the presented system, we estimate that setting $V_{DS} = 8\text{V}$ and V_{GS} in the range of maximum $\pm 15\text{V}$ (30V clearance), would lead I_{DS} to occur in the range of 10^{-9} to 10^{-6}A , which is a reasonable tradeoff between the sensor's sensitivity and the achievable on-chip high voltage, as will be further discussed in section III.A.

Fig. 3. Ambipolar OFET transfer characteristics in the saturation regime obtained for holes (left) and electrons (right) [6].

As can also be noticed in Fig. 3, the I_{DS} transfer characteristics have hysteresis. Recent research [4] demonstrated that this hysteresis could be used to improve the OFET's gas selectivity. Furthermore, some of our OFET are ambipolar with well-balanced hole and electron mobilities. This amipolar selectivity doubles the set of parameters that could be used for gas detection with positive impact on gas selectivity, which is one motivation for being able to apply both positive and negative V_{GS} as mentioned above (also see section III.D).

Therefore, the integrated instrumentation system should feature the following functionalities: 1) sweep the gate voltage V_G while maintaining V_D and V_S constant, and 2) convert I_{DS} into a digital signal for further advanced data processing (gas signature recognition for example).

As basic as they might appear, these functionalities yet imply the development of several complex mixed-signal sub-functions as developed in the next section.

III. SYSTEM ARCHITECTURE

The architecture of the whole system is presented in Fig. 4. It is composed of a mixed-signal HV CMOS ASIC and an FPGA SoC. The ASIC is in charge of generating independent OFET's biasing voltages (V_G , V_D , V_S) enabling multiple V_{DS} and V_{GS} configurations, generating high voltages from the single LV (5V) supply, converting the OFET's I_{DS} current into an integrated differential voltage, and performing analogue-to-digital conversion of the differential voltage. As for the FPGA

SoC, it is in charge of sequencing the whole system (multiple clocks generation, V_G control, and acquisition and readout cycles), handling and processing the ADC dataflow, and communicating with user PC

Fig. 4. Synoptic view of the system's architecture.

Note that, although the whole system could have been implemented onto one single integrated chip, for flexibility and rapid prototyping reasons we deliberately implemented the digital part onto an FPGA target.

A. High-voltage power supply (generator)

The required high voltages are generated on-chip from the single 5V supply voltage. For that purpose, we designed 2 latched charge pumps (LPCs), using the design methodology and dimensioning tool described in [7]. The LPCs' specifications are: $28\text{V} - 23.2\mu\text{A}$ for LCP1, and $40\text{V} - 14\mu\text{A}$ for LCP2. Both LPCs use a 20MHz clock frequency. They are used to supply the system's HV guard ring (LCP2) and 3 HV amplifiers (HVAs) that generate the OFET's biasing, i.e. LCP1 for V_D and V_S , and LCP2 for V_G as described below.

B. High-voltage amplifiers

The role of the HVAs presented in Fig. 5 is to generate the OFET's biasing voltages (V_G , V_D , V_S) from bandgap-referenced input voltages, and also to operate conversion of its current, I_{DS} , in order to enable LV readout.

Fig. 5. HVA bloc and related signals.

The HVAs are based on the Miller OTA topology [8] in non-inverting amplifier configuration as presented in Fig. 6. The differential input stage is powered by the LV supply ($V_{DD_LV} = 5\text{V}$) and is thus exclusively composed of LV transistors (supporting maximum voltage of 5.5V in the chosen technology). It is followed by an HV gain stage powered by the LPCs (V_{DD_HV}). The partition between LV and HV voltages is guaranteed by the HV transistor M_N whose gate voltage is bound to V_{DD_LV} , thus ensuring the voltages never exceed V_{DD_LV} on the LV transistors. All stages are biased through cascaded current sources.

Fig. 6. Non-inverting amplifier HVA topology.

Since the system is single-supply powered, to get $V_{DS} = 8V$, V_S and V_D are set to 16V and 24V respectively, with 1.65V input voltage, which yields gains of 9.7 and 14.55 respectively. For V_D and V_S , the reference voltage V_{ref} (Fig. 6) of the related HVAs is set to ground. Concerning V_G , it should vary on a range of maximum $\pm 15V$ around either 16V or 24V depending on the measured current (electrons or holes) of the OFET (p-type, n-type or amipolar). Therefore, the V_{ref} input of the V_G HVA can be adjusted according to the desired mid-range point (i.e. 16V or 24V). The input voltage of the V_G HVA is delivered by a bandgap-referenced 5-bit DAC with $\pm 1V$ dynamics around 1.65V, which yields a gain of 15. Note that V_{ref} should also compensate for the DAC's mid-range point (i.e. 1.65V).

The OFET current, I_{DS} , is processed by the LV readout chain presented in section XX. As shown in Fig. 7, this is made possible by connecting the V_S HVA to a cascoded current mirror that copies I_{DS} from HV to LV while maintaining V_S constant on the OFET.

Fig. 7. HV to LV conversion of I_{DS} .

Since the input voltages are rather low (i.e. 1.65V for V_D and V_S , 0.65V to 2.65V for V_G) the HVAs have been designed so as to support 0.5V to 3.5V common mode with 1.65V nominal operating point. The HV stages of the V_D and V_S HVAs have 28V supply (LCP1) and 0.2V to 26.5V output dynamics. As for the V_G HVA, it has 40V supply (LCP2) and 0.2 to 39V output dynamics in order to support the $\pm 15V$ sweep for the various configurations. All HVAs have 200 kHz GBW, which is largely sufficient considering the implied gains and the very low OFET's operating frequency, around 0.5Hz.

C. Low-voltage integration chain and analog to digital conversion

The LV copy of I_{DS} , delivered by the current mirror, is converted into a differential voltage by means of the current-to-voltage integration chain presented in Fig. 8, and which also acts as an anti-aliasing filter. The fully differential amplifier has $\pm 1V$ output dynamics, and the overall gain allows to convert currents ranging from $10^{-9}A$ to $10^{-6}A$. The signal is then converted into a 1MHz bit train by a 12-bit resolution second order $\Sigma\Delta$ modulator with $\pm 1V$ input dynamics [9].

Fig. 8. I_{DS} readout and analog-to-digital conversion chain.

D. Digital control and processing

The whole system is controlled by a digital SoC implemented on an Altera[®] FPGA. It features a NIOS II processor that is mainly in charge of handling the data delivered by the ADC (storage and transfer to user PC), and configuring the various operating modes of the real-time blocs, namely a sequencer and finite impulse response (FIR) filter. These real-time blocs have been designed in VHDL language. The sequencer generates the various clocks and control signals (LCPs, $\Sigma\Delta$ modulator, FIR enable, DAC cycle start, etc.) and, above all, controls the DAC sequence to generate specific V_G pattern as presented below.

• V_G pattern control

The gate voltage V_G is controlled by the 5-bit DAC (i.e. 32 values with 0.93V step quantum), which allows 64 steps cycles (V_G increasing and decreasing). In addition to biasing considerations, the efficiency of the OFET's response to gas exposure depends on its operating speed. In particular, better selectivity is achieved when the sweep cycle of V_G has above 1 minute duration. Therefore, the initial sweep cycle consisted in generating a stair-shaped V_G pattern by continuously incrementing and decrementing the DAC value at 0.5Hz rate, leading to 128s cycle duration. Yet, as can be noticed on Fig. 2, this pattern causes a drift of the quiescent I_{DS} , i.e. when gas exposure stops, which implies systematic recalibration of the sensor prior to measurement. Experimental research on that topic shows that this phenomenon might be related to charge trapping within the OFET's active zone and is currently further investigated. The solution to circumvent this issue is presented in Fig. 9. It consists in applying the opposite voltage after each step of V_G . This causes "de-trapping" of the corresponding charge specie (electrons or holes) depending on the OFET's type. The total cycle duration is then around 250s. With this pattern, the charge de-trapping occurs without hysteresis loss. This is due to the kinetic difference behind the de-trapping (fast) and hysteresis (slow) phenomena.

Fig. 9. DAC control pattern Modelsim® simulation.

- ADC process and FIR filter

In case of a unipolar OFET (n-type or p-type), the ADC sampling is triggered for each V_G step. In case of an ambipolar OFET, the de-trapping phase also corresponds to the activation of the opposite specie's current and the sampling is thus triggered on both (positive and negative) V_G phases. The ADC process is triggered 20ms after each V_G step in order to ensure steady I_{DS} . The 1MHz bit stream delivered by the $\Sigma\Delta$ modulator is fed to a 1024-bit RAM corresponding to the number of coefficients of a custom multiplier-free FIR filter [10]. Once the RAM is full (i.e. after 1ms) the FIR calculation, consisting in 1024 accumulations operated at 20MHz, is triggered in order to deliver 12-bit samples.

IV. EXPERIMENTAL RESULTS

A prototype circuit has been designed and fabricated in AMS 0.18 μ m HV-CMOS technology. Fig. 10 shows a micrograph of the ASIC and a picture of the whole system featuring the ASIC test board connected to an Altera® Cyclone II development board.

Fig. 10. Chip micrograph (left) and system picture (right).

The ASIC is power by a 5V (LV) supply, with 300 μ A total current consumption. The measurements performed on the charge pump LCP1 revealed 27.9V – 23.8 μ A, which is in good accordance with the specifications. The measurements on LCP2 revealed 37.9V – 13 μ A, which is slightly under the expected performances. This compels us to lower V_D and V_S to 14V and 22V respectively, and to reduce V_G in the ± 13 V range when its mid-range point is set to 22V. Fig. 11 shows the measured V_G cycle when the mid-range point set to 16V and the V_G range is ± 14 V.

Fig. 11. Experimental V_G cycle with mid-range point set to 16V.

Fig. 12 shows results obtained from a unipolar OFET operating as a gas sensor for various ethanol concentrations. Further experiments are currently under progress.

Fig. 12. Transient I_{DS} and mobility response of a unipolar P3HT OFET exposed to 2000ppm to 500ppm of ethanol an alternating polarity mode V_G .

V. CONCLUSION

An instrumentation system dedicated to OFET-based sensors has been presented. It features a 5V single-supply 0.18 μ m HV CMOS technology prototype that has been experimentally validated. The system is now fully operational for further investigation on various types of OFET devices. The validation of its concept now opens the way to the next stage towards mobile applications, i.e. full integration, including on-chip (ASIC) digital processing and OFET interfacing.

REFERENCES

- [1] H. Zheng, B. Ramalingam, V. Korampally, and S. Gangopadhyay, "Large sensitivity enhancement in semiconducting organic field effect transistor sensors through incorporation of ultra-fine platinum nanoparticles," *Appl. Phys. Lett.*, vol. 103, no. 19, p. 193305, 2013.
- [2] H. Zheng and S. Gangopadhyay, "Molecularly imprinted organic transistor-based sensor for selective trace chemical vapor detection," *2015 Transducers - 2015 18th International Conference on Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS)*, Anchorage, AK, 2015, pp. 634-637.
- [3] J. Huang, J. Miragliotta, A. Becknell, and H. E. Katz, "Hydroxy-terminated organic semiconductor-based field-effect transistors for phosphonate vapor detection," *J. Am. Chem. Soc.*, vol. 129, no. 30, pp. 9366-9376, 2007.
- [4] P. Liennerth, S. Fall, P. Lvque, U. Soysal and T. Heiser, "Improving the selectivity to polar vapors of OFET-based sensors by using the transfer characteristics hysteresis response", *Sensors and Actuators B*, vol. 225, pp. 90-95, 2016.
- [5] P. Liennerth, "Elaboration and characterization of field-effect transistors based on organic molecular wires for chemical sensing applications", PhD thesis, Universit de Strasbourg, 2014.
- [6] A. Mirloup, N. Leclerc, S. Rhin, T. Bura, R. Bechara, A. Hbraud, P. Lvque, T. Heiser and R. Ziessel, "A deep-purple-grey thiophene-benzothiadiazole-thiophene BODIPY dye for solution-processed solar cells", *New, J. Chem.*, vol. 38, pp. 3644-3653, 2014.
- [7] J. Heitz, V. Frick, N. Dumas, L. Hbrard, C. Lallement, "Modeling and Optimization of a Latched Charge Pump Loaded by a Resistive Circuit," *Analog Integrated Circuits and Signal Processing*, Springer Verlag, vol. 83, no. 3, 2015, pp. 353-367.
- [8] J. H. Huijsing, *Operational amplifiers theory and design*, Springer, pp. 400-402. 2001.
- [9] R. Schreier and G. C. Temes, *Understanding Delta-Sigma Data Converters*, IEEE Press/Wiley, 2005.
- [10] V. Frick, F. Dadouche, H. Berviller, "Adjustable Nyquist-rate System for Single-Bit Sigma-Delta ADC with Alternative FIR Architecture," *International Journal of Electronics*, Taylor & Francis, 2015, vol. 103, no. 9, pp. 1593-1606.